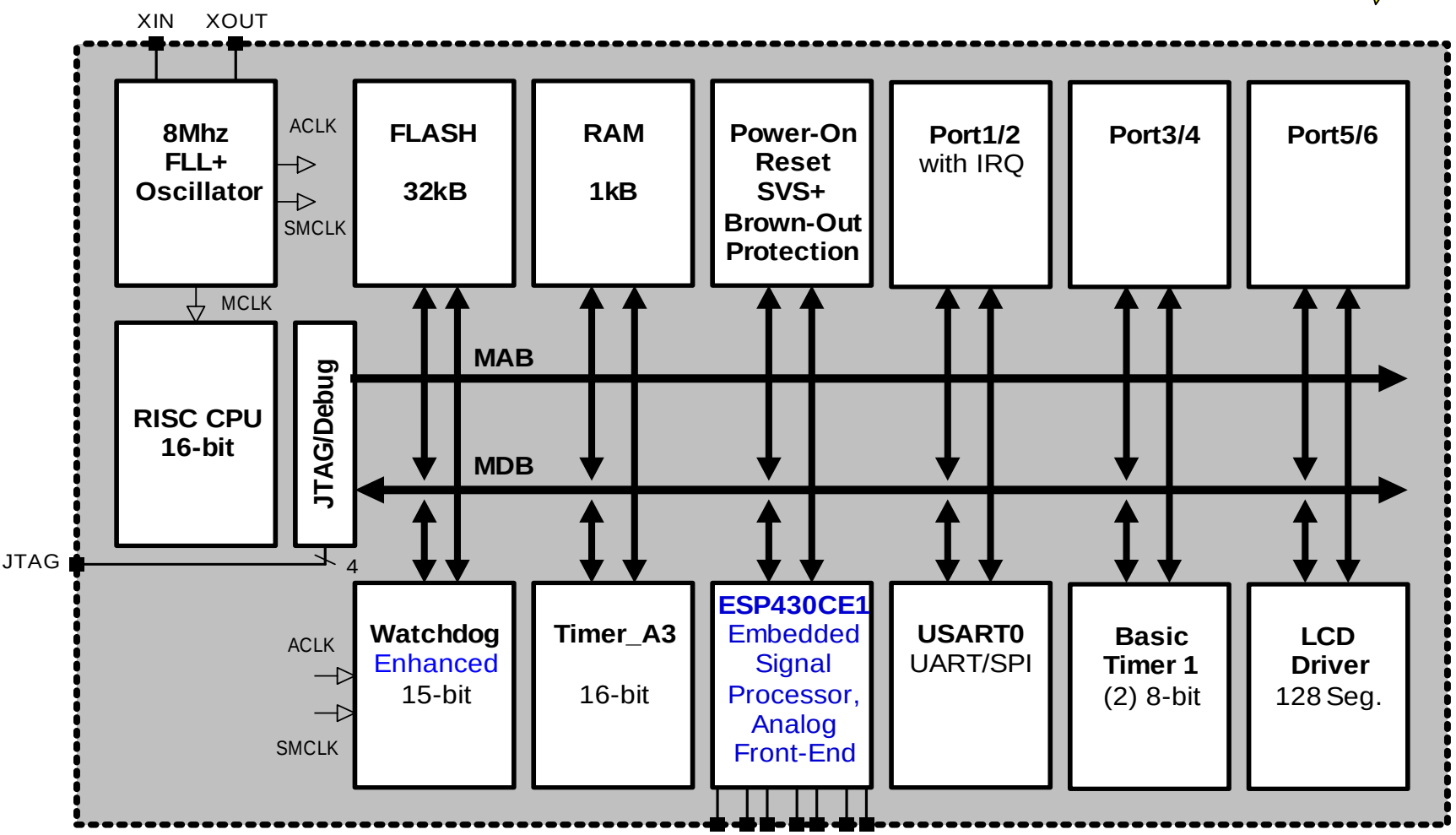
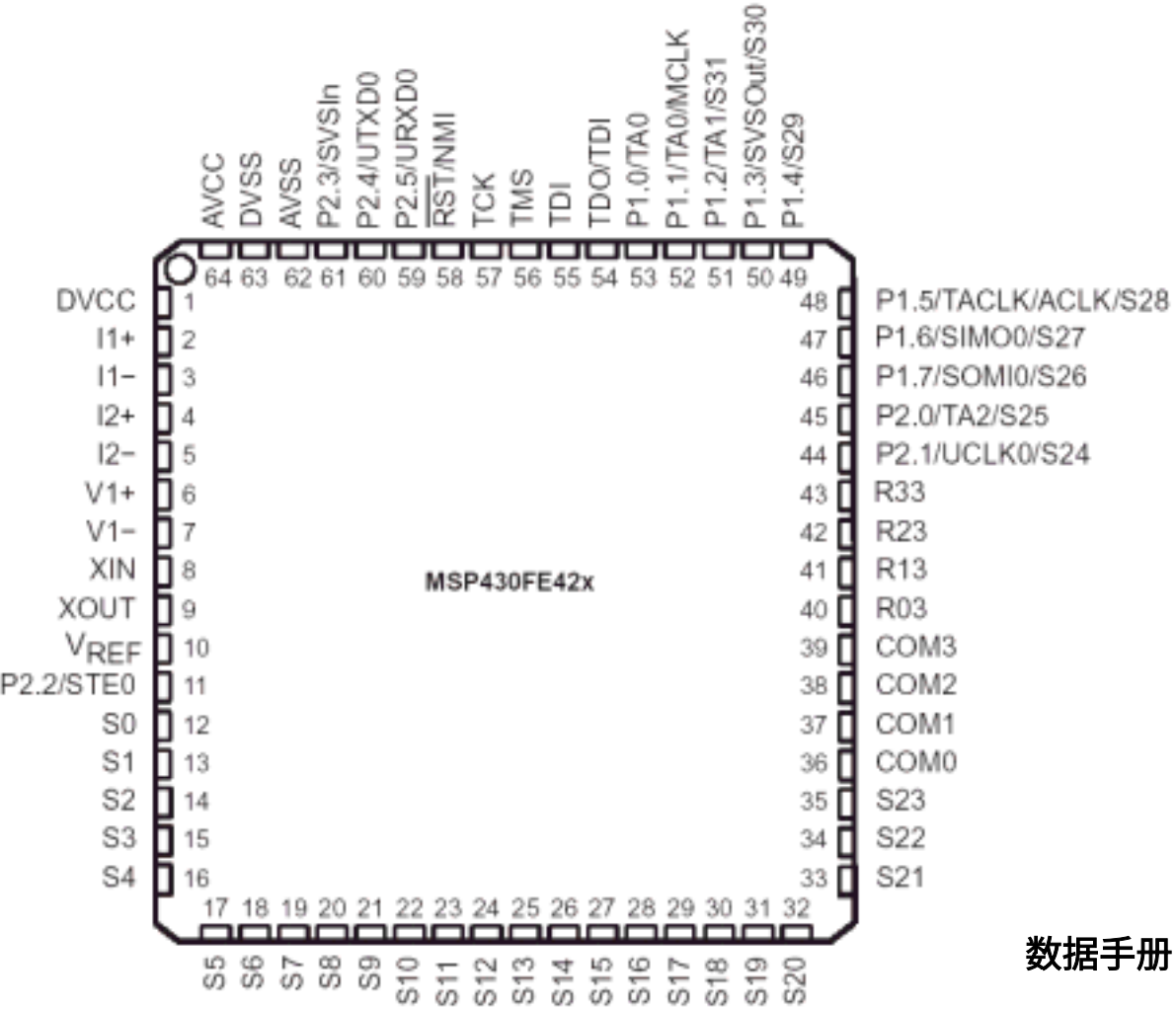
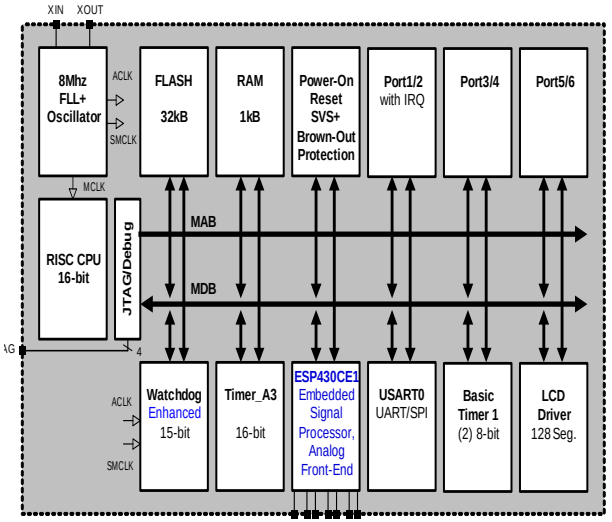
MSP430FE427

Preview



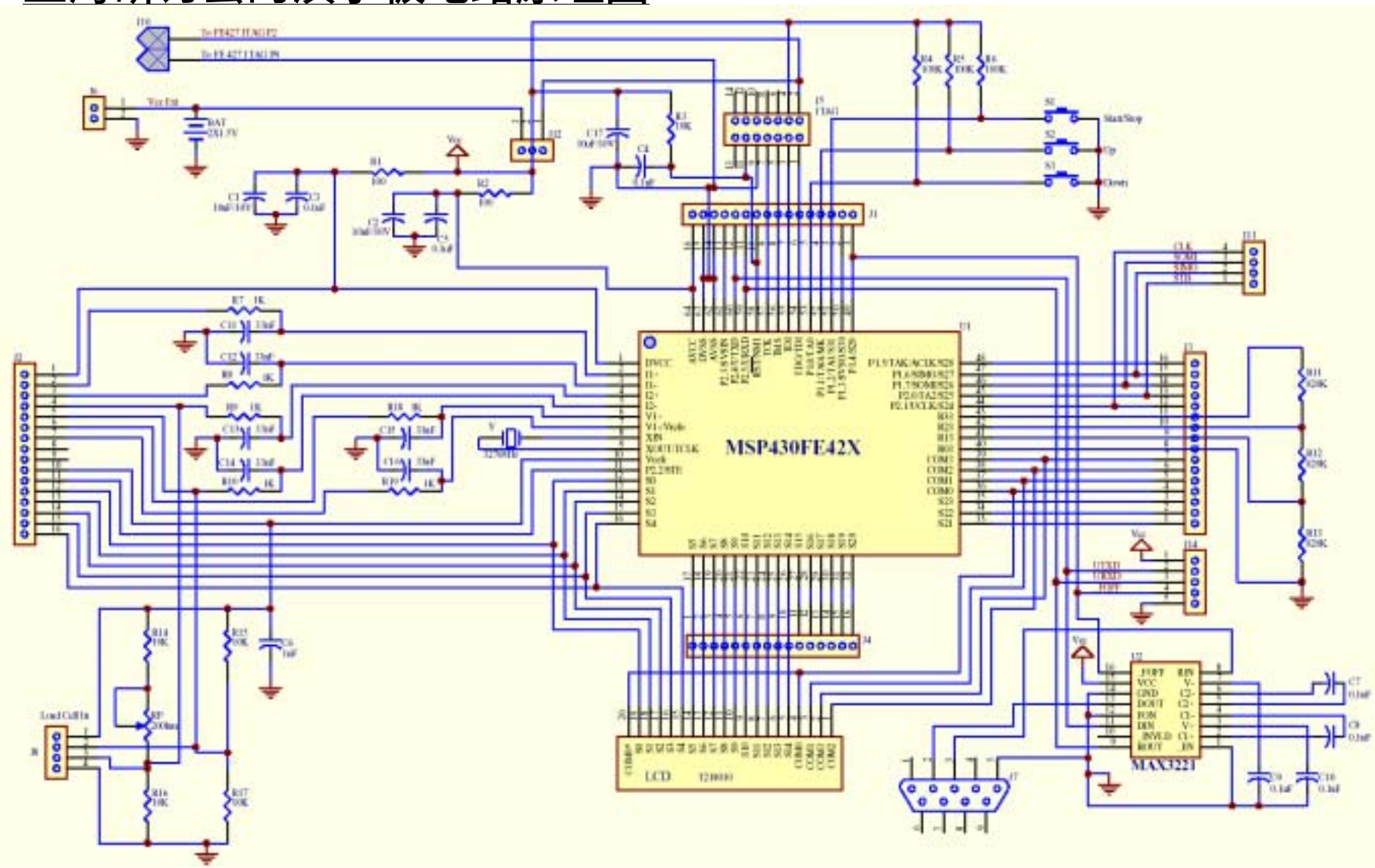




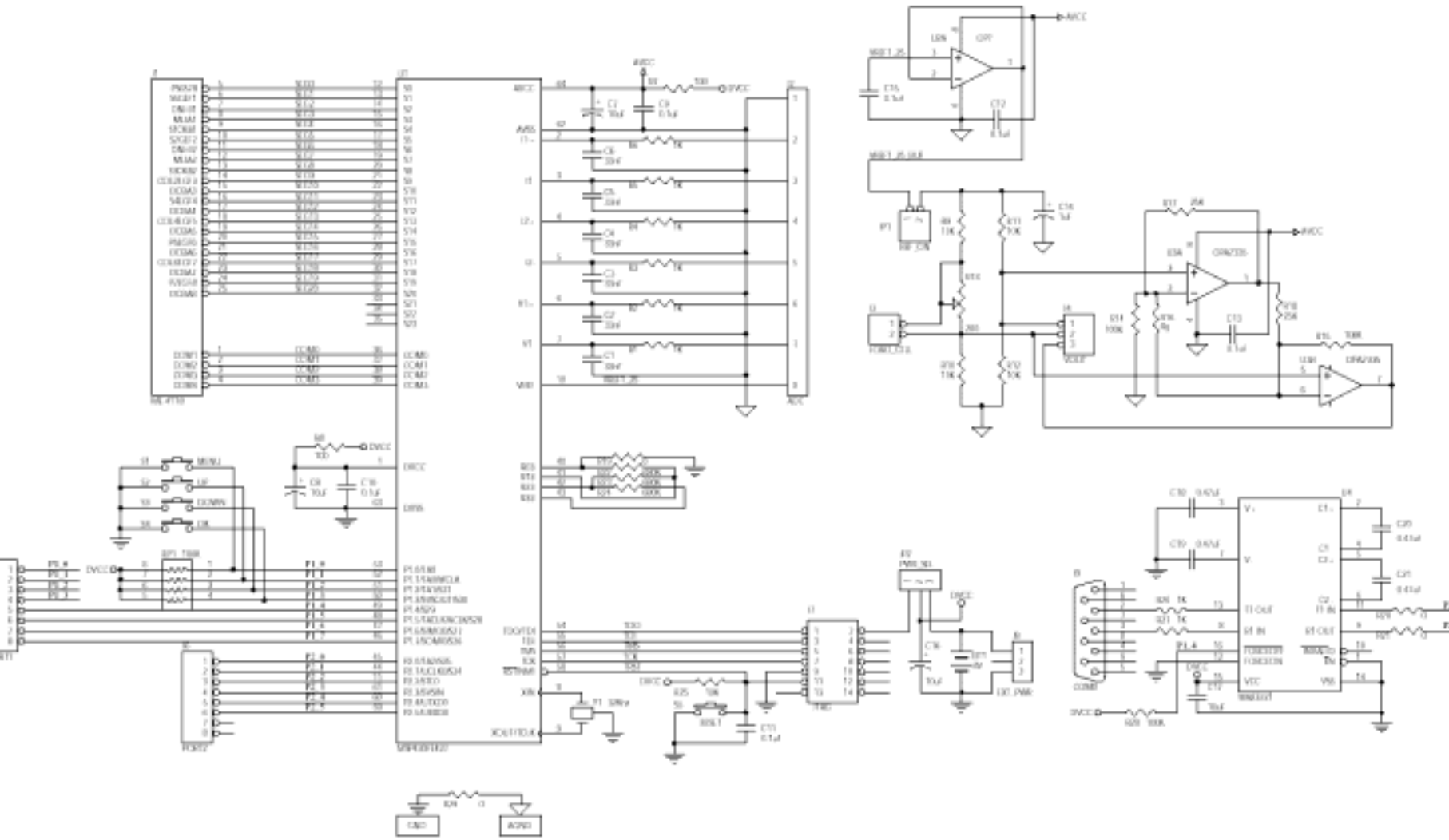
数据手册：MSP430FE427.pdf

用户指南：F4XX_Users_guide_SLA056C

上海研讨会的演示板电路原理图

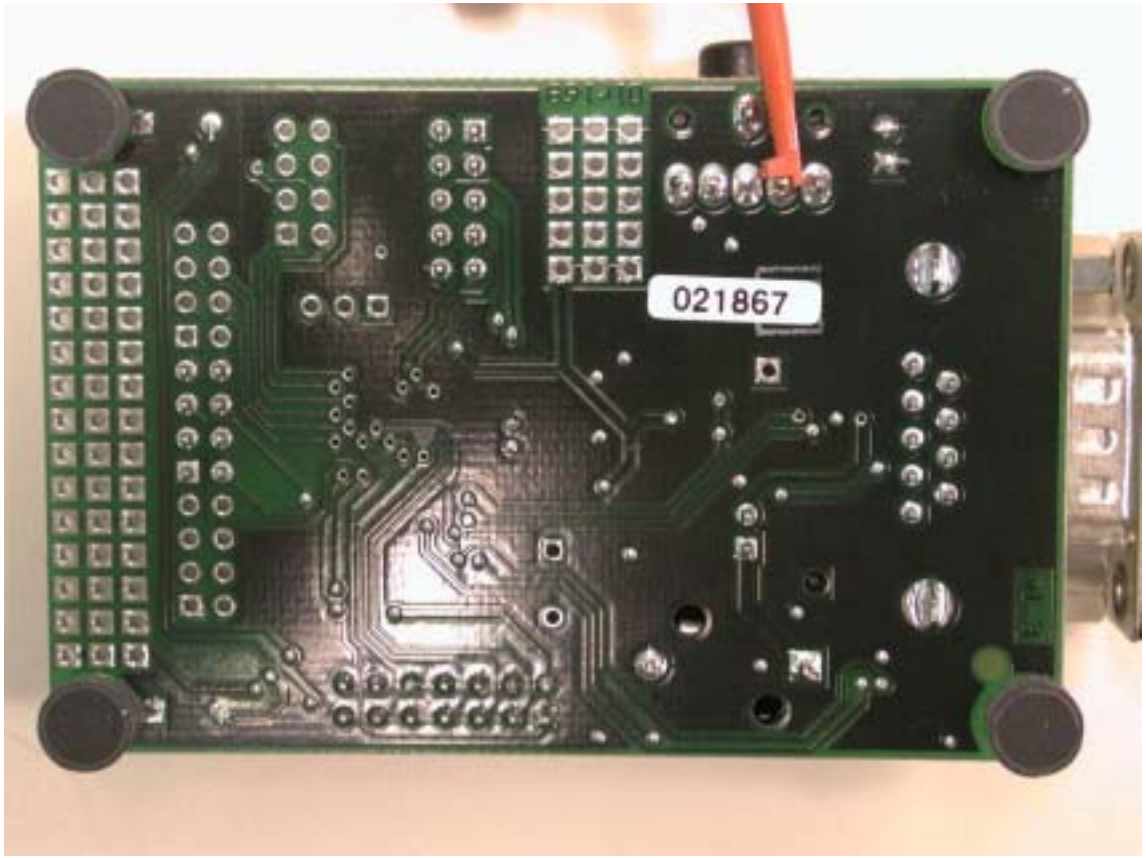


台北研讨会的演示板电路原理图



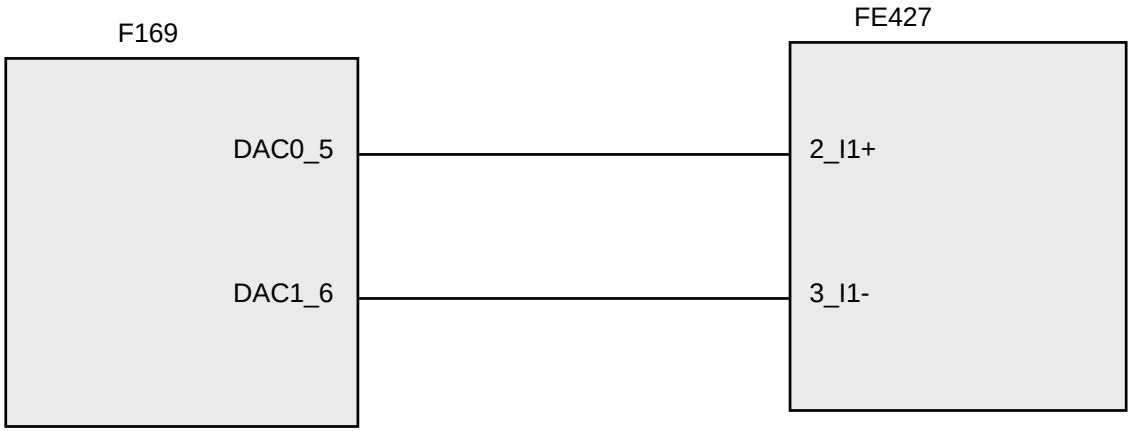
Project: WaveMachine (F169演示板)

Project: Voltmeter RMS (FE427演示板)

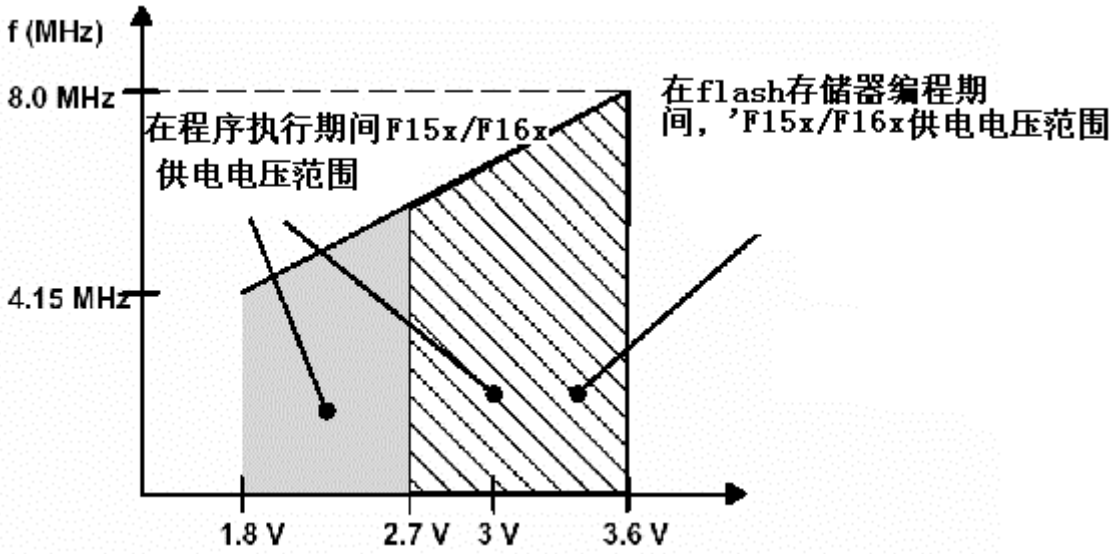


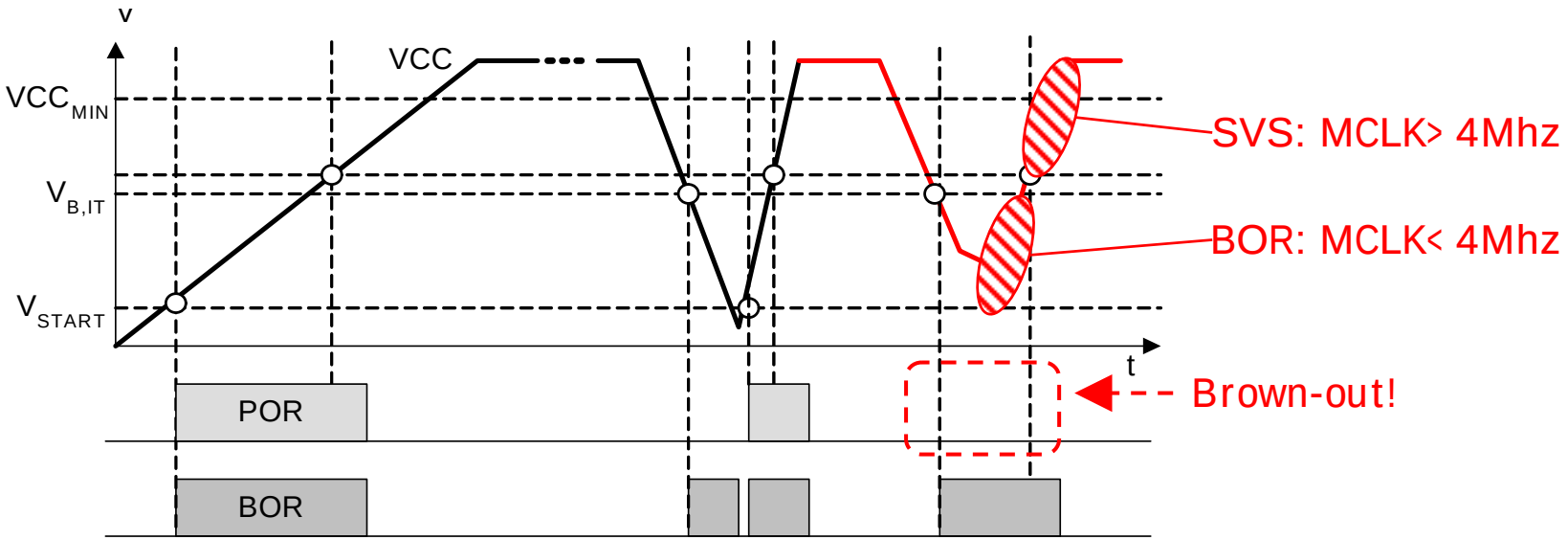
Project: WaveMachine (F169演示板)

Project: Voltmeter RMS (FE427演示板)



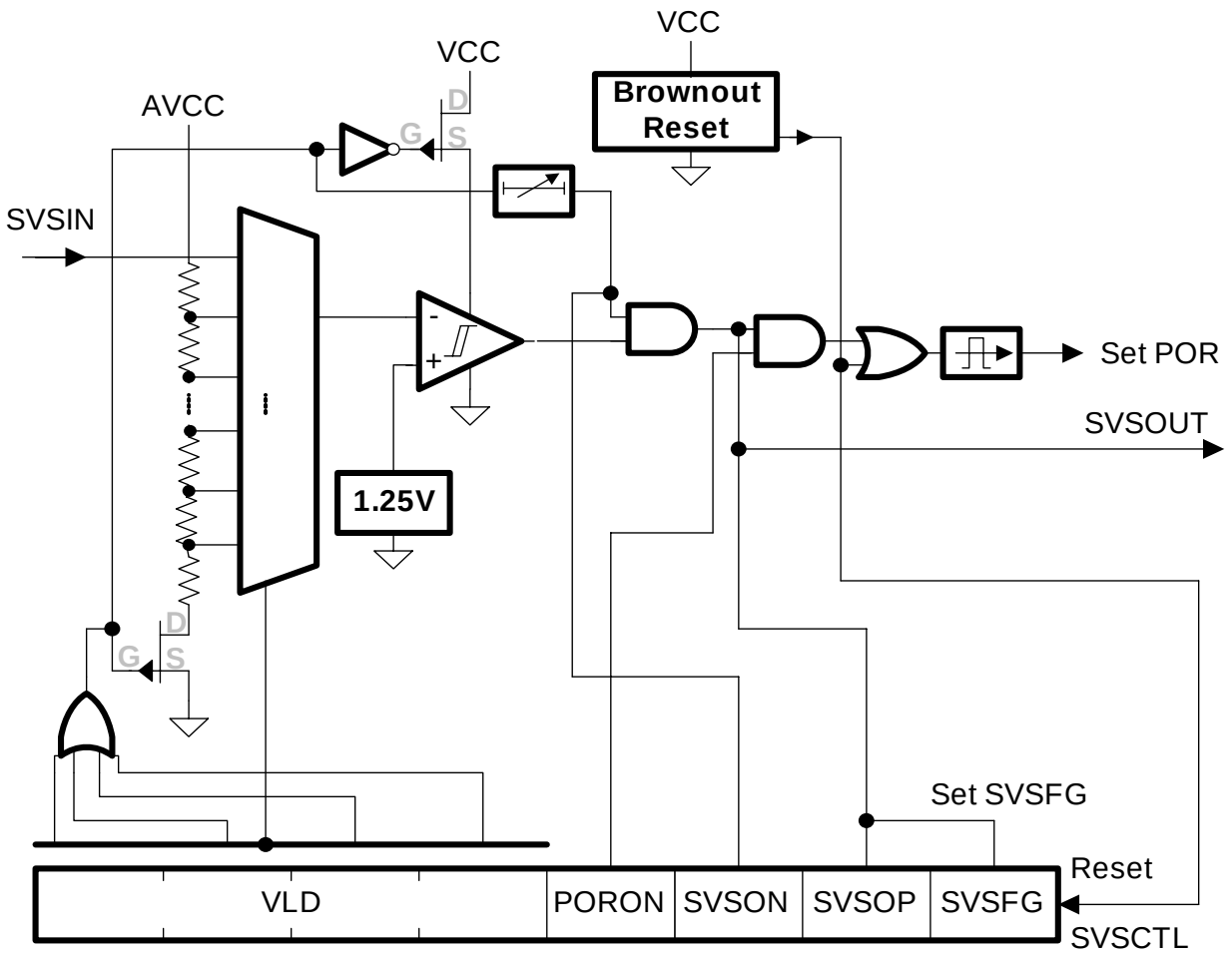
超低功耗 BOR


f (MHz)
8.0 MHz
4.15 MHz
在程序执行期间F15x/F16x
供电电压范围
在flash存储器编程期
间，'F15x/F16x供电电压范围
1.8 V
2.7 V
3 V
3.6 V


v
VCC
VCC_MIN
V_B,IT
V_START
t
POR
BOR
SVS: MCLK> 4Mhz
BOR: MCLK< 4Mhz
Brown-out!

SVS

- AVCC 监控
- 可选择POR的产生
- 可通过软件读取SVS比较器的输出
- 低电压条件锁定，且软件可存取
- 14 个可选择的门限电平
- 外部电压可通过外部通道监控



VLDx Bit 电平检测。SVS上3位选择门限电平。以下为各个参数的详细数据表：

7-4

0000	SVS is off	1100	3.35 V
0001	1.9 V	1101	3.5 V
0010	2.1 V	1110	3.7 V
0011	2.2 V	1111	比较外部输入电压SVSin和1.2v
0100	2.3 V		
0101	2.4 V		
0110	2.5 V		
0111	2.65 V		
1000	2.8 V		
1001	2.9 V		
1010	3.05		
1011	3.2 V		

```
SVSCTL |= (SVSON | 0x60);

while ((SVSCTL & SVSOP));

SVSCTL |= PORON;
```

PORON Bit3 POR开启。该位使能SVSFG标志位，引起一个POR设备重启。
0 SVSFG不引起一个POR
1 SVSFG引起一个POR

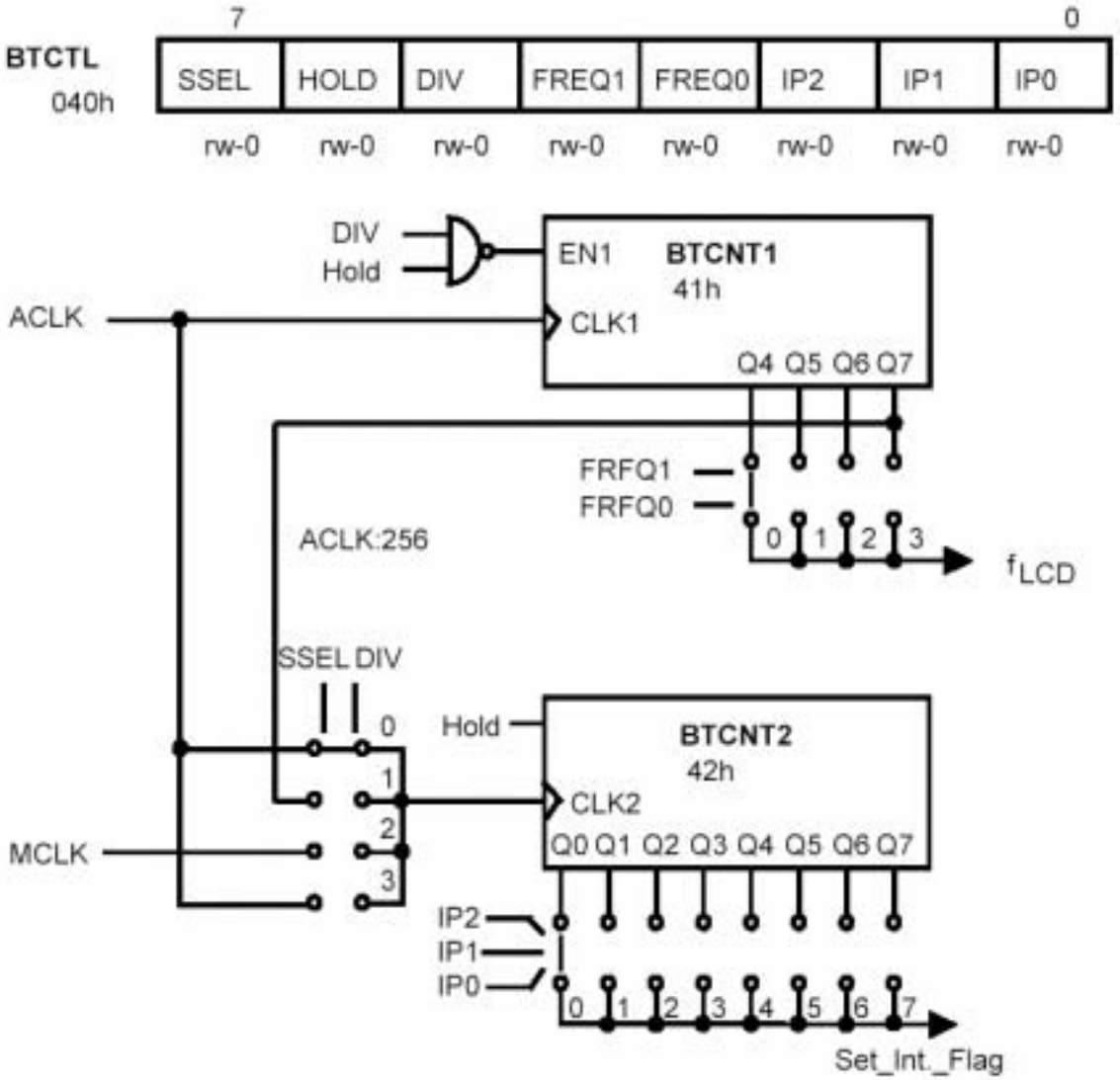
SVSON Bit2 SVSON开启。该位反映SVS运行状态。该位不能开启SVS。通过设置VLDx>0开启SVS.
0 SVS 开启
1 SVS 关闭

SVSOP Bit1 SVS输出。该位反映SVS比较器的输出值。
0 SVS比较器输出高电平
1 SVS比较器输出低电平

SVSFG Bit0 SVS标志位。该位表示低压状态。在电压状态后SVSFG维持原先设置直到由软件重启。

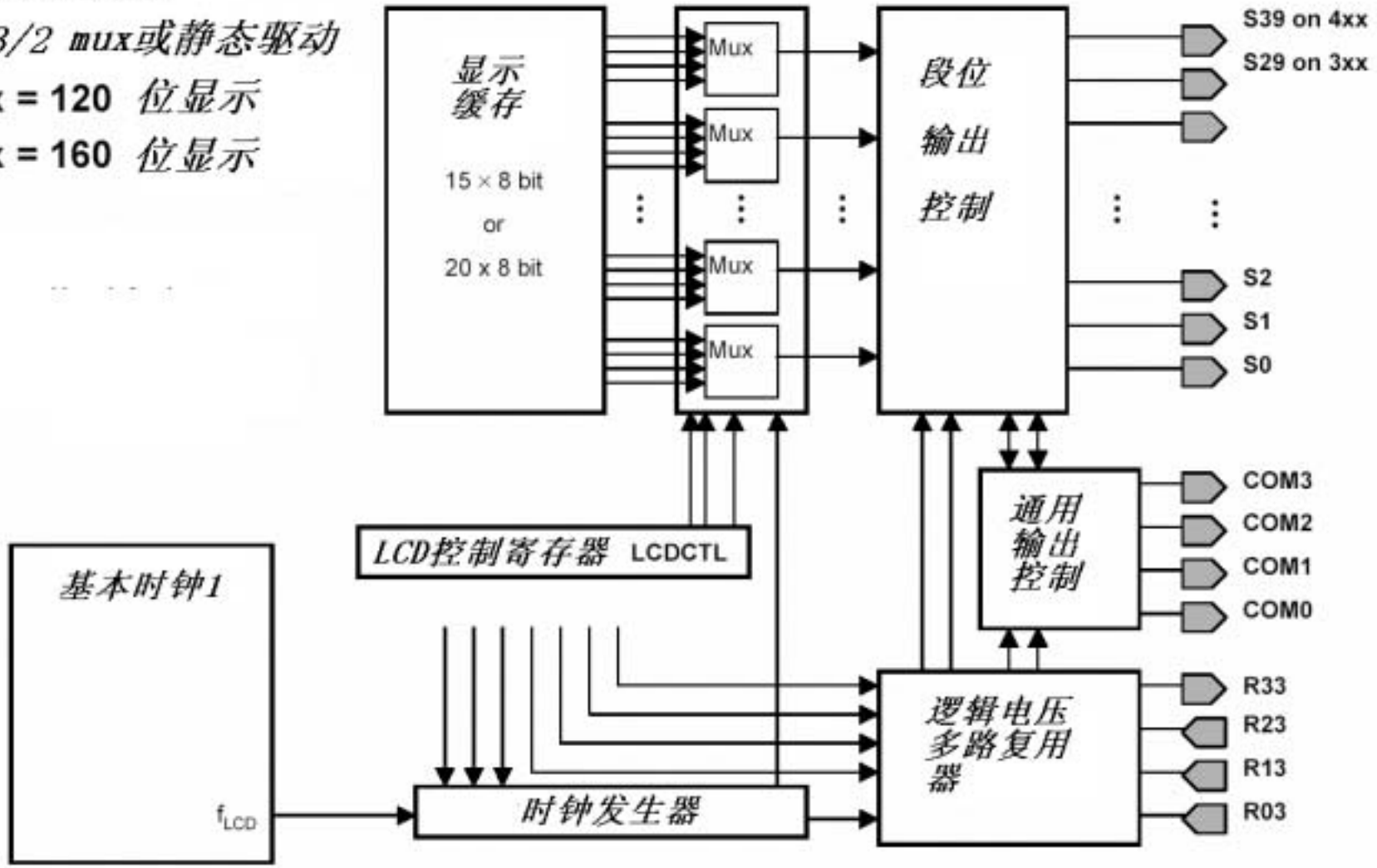
基本时钟

- 一个16位 或 两个8位定时器
- 支持实时时钟中断
- LCD的驱动频率

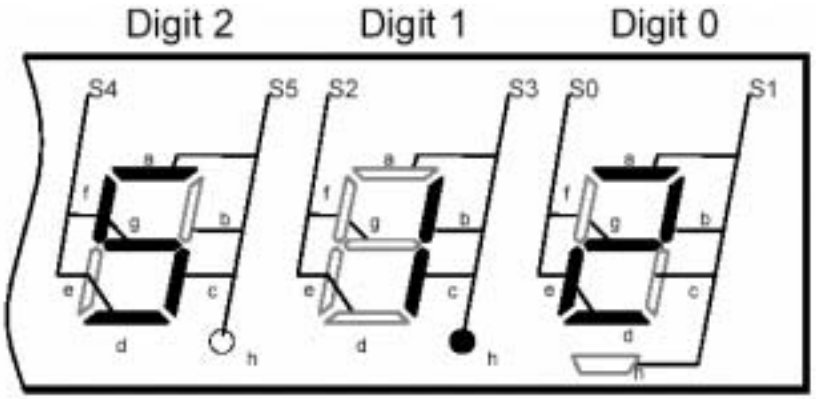


LCD Module #1

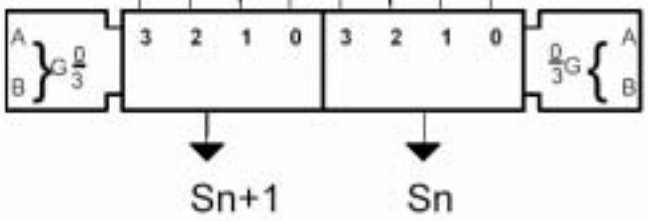
- 极低的功耗
- 4/3/2 mux或静态驱动
- 3xx = 120 位显示
- 4xx = 160 位显示



LCD 模块 #2



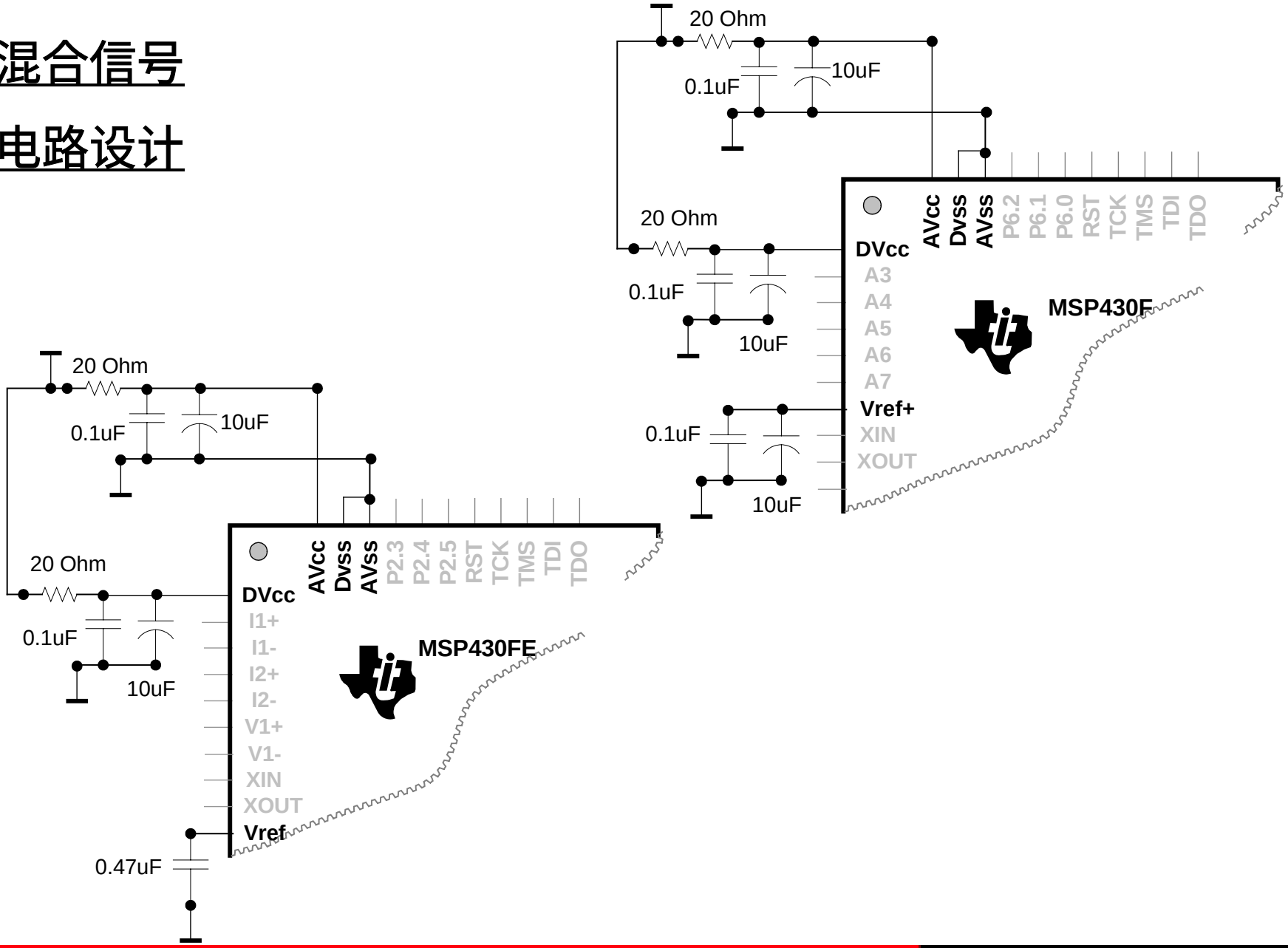
COM	3	2	1	0	3	2	1	0	
03Fh	a	b	c	h	f	g	e	d	n = 28
035h	a	b	c	h	f	g	e	d	8
034h	a	b	c	h	f	g	e	d	6
033h	a	b	c	h	f	g	e	d	4
032h	a	b	c	h	f	g	e	d	2
031h	a	b	c	h	f	g	e	d	0




```
; ***** 定义段值

a           equ     80h
b           equ     40h
c           equ     20h
d           equ     01h
e           equ     02h
f           equ     08h
g           equ     04h
h           equ     10h

;
; 为每个数字定义显示的段值

Table   db    a+b+c+d+e+f       ; 0
        db    b+c               ; 1
;             • • •
        db    a+b+c+d+f+g       ; 9

;
; 装载要显示的三个数字的二进制值
;

        mov.b   Table(R5),&31h  ; 2 in R5, S0/S1
        mov.b   Table(R5),&32h  ; 1 in R5, S2/S3
        mov.b   Table(R5),&33h  ; 5 in R5, S4/S5
        bis.b   #10h,&32h       ; 十进制小数点
```

混合信号

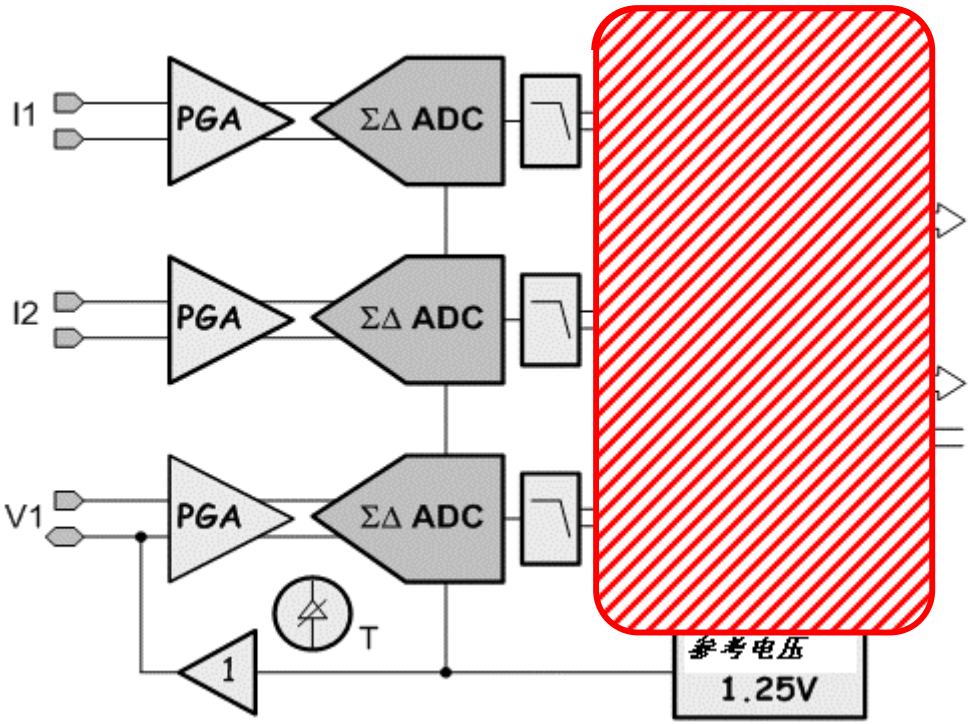
电路设计


20 Ohm
0.1uF
10uF
20 Ohm
0.1uF
10uF
0.1uF
10uF
AVcc
Dvss
AVss
P6.2
P6.1
P6.0
RST
TCK
TMS
TDI
TDO
DVcc
A3
A4
A5
A6
A7
Vref+
XIN
XOUT
MSP430F
20 Ohm
0.1uF
10uF
20 Ohm
0.1uF
10uF
AVcc
Dvss
AVss
P2.3
P2.4
P2.5
RST
TCK
TMS
TDI
TDO
DVcc
I1+
I1-
I2+
I2-
V1+
V1-
XIN
XOUT
Vref
MSP430FE
0.47uF

ESP430 – 复合信号概念

ESPCTL &= ~BIT0;

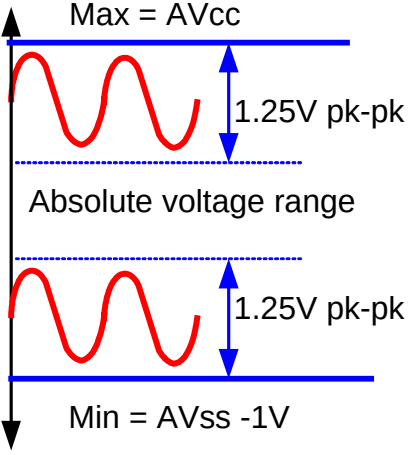
- 嵌入式信号处理器 - ESP430
- 性价比较高的混合信号处理
- 逻辑信号和数字信号处理合二为一
- 返回能量，功率，电压，电流

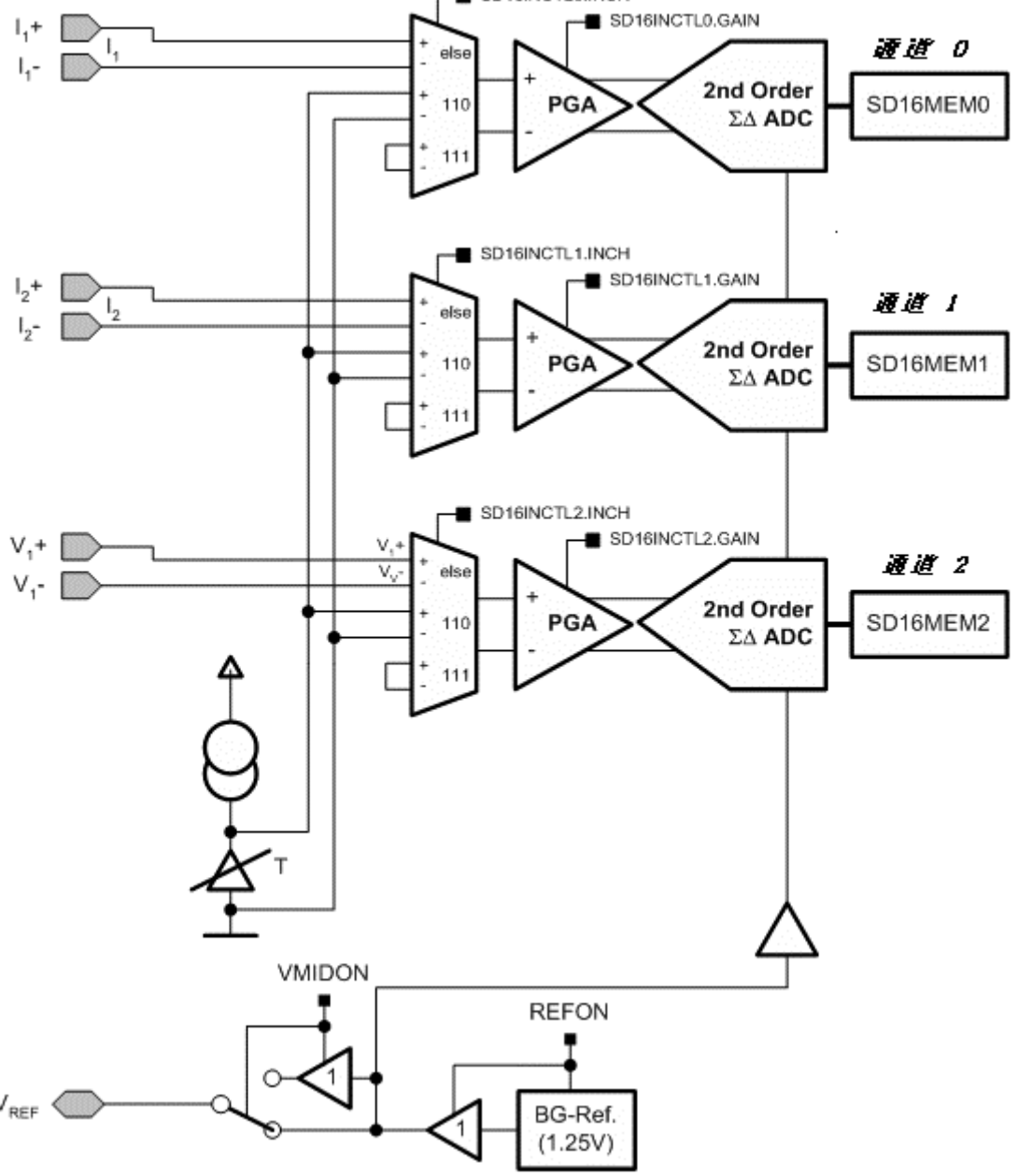


SD16

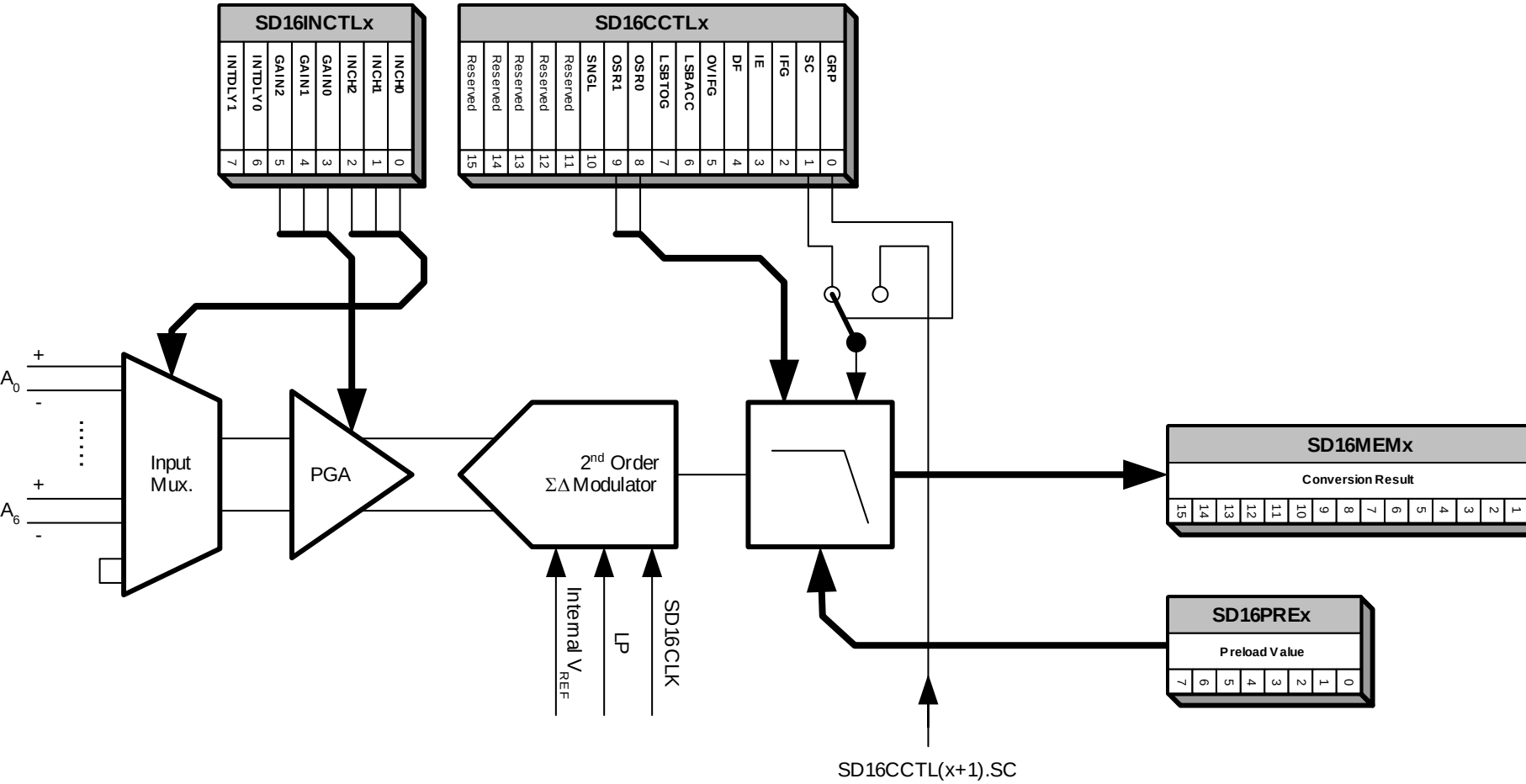
输入

范围

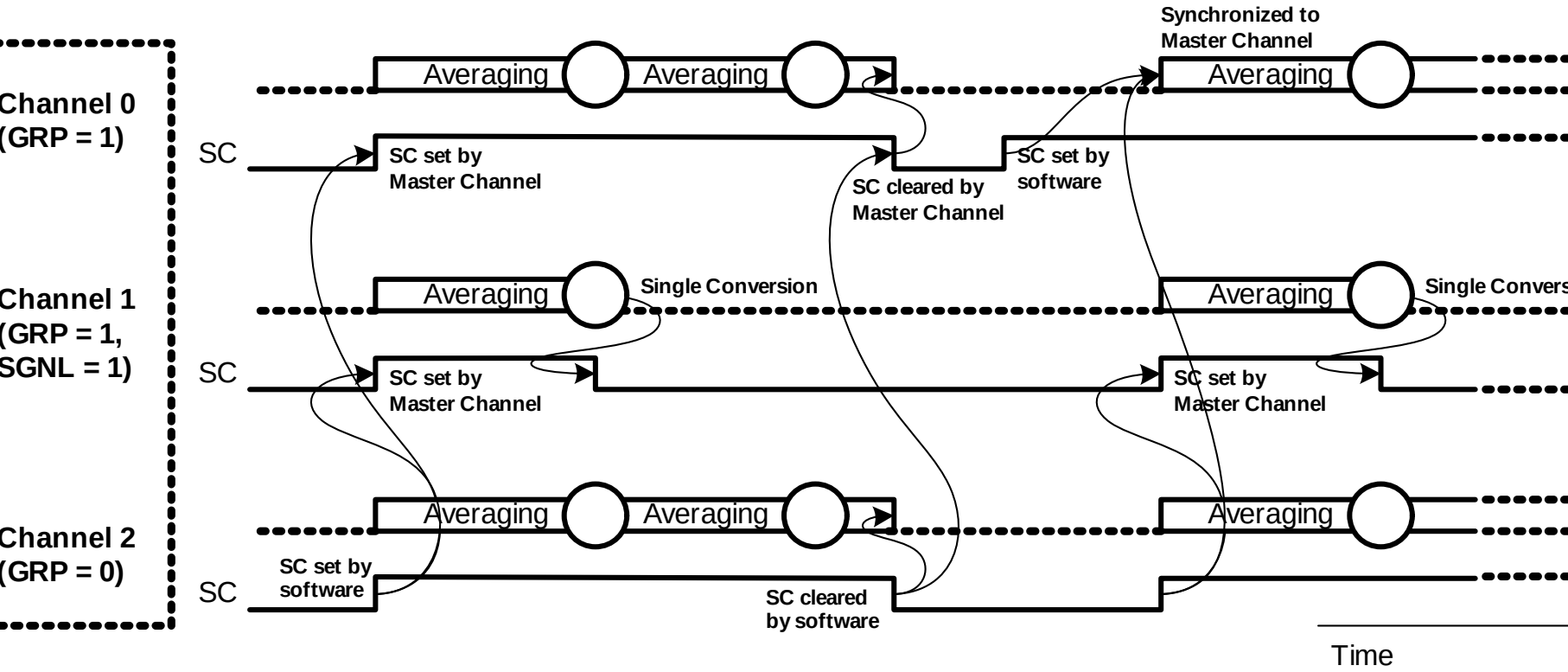

Max = AVcc
1.25V pk-pk
Absolute voltage range
1.25V pk-pk
Min = AVss -1V


I1+
I1-
I1
SD16INCTL0.GAIN
else
110
111
PGA
2nd Order
ΣΔ ADC
通道 0
SD16MEM0
I2+
I2-
I2
SD16INCTL1.INCH
SD16INCTL1.GAIN
通道 1
SD16MEM1
V1+
V1-
SD16INCTL2.INCH
SD16INCTL2.GAIN
通道 2
SD16MEM2
T
VMIDON
REFON
VREF
1
BG-Ref.
(1.25V)

SD16 信号控制


SD16INCTLx
INTDLY1 INTDLY0 GAIN2 GAIN1 GAIN0 INCH2 INCH1 INCH0
7 6 5 4 3 2 1 0
SD16CCTLx
Reserved Reserved Reserved Reserved Reserved SNGL OSR1 OSR0 LSBTOG LSBACC OVIFG DF IE IFG SC GRP
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
A0
A6
Input Mux.
PGA
2nd Order ΣΔ Modulator
Internal VREF
LP
SD16CLK
SD16MEMx
Conversion Result
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SD16PREx
Preload Value
7 6 5 4 3 2 1 0
SD16CCTL(x+1).SC

SD16 通道同步


Channel 0
(GRP = 1)
Channel 1
(GRP = 1,
SGNL = 1)
Channel 2
(GRP = 0)
SC
SC
SC
Averaging
Averaging
Averaging
Averaging
Averaging
Averaging
Averaging
Synchronized to
Master Channel
SC set by
Master Channel
SC cleared by
Master Channel
SC set by
software
Single Conversion
SC set by
Master Channel
SC set by
Master Channel
Single Convers
SC set by
software
SC cleared
by software
Time

SD16 控制

SD16CTL

0100h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							LP	DIV		SSEL		VMID ON	REF ON	OVIE	Res.
r0	r0	r0	r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r0

SD16CTL = 0x800 + SD16SSEL_1

| SD16DIV_1

| SD16VMIDON

| SD16REFON;

REFON 打开Vmid缓冲区.如果中间电压没有使用，则关闭以节省能量.注意：参考电压用作中间电压

VMIDON 打开内部参考电压. 如果未使用参考电压则关闭以节省能量。.

SSEL 选择时钟源.

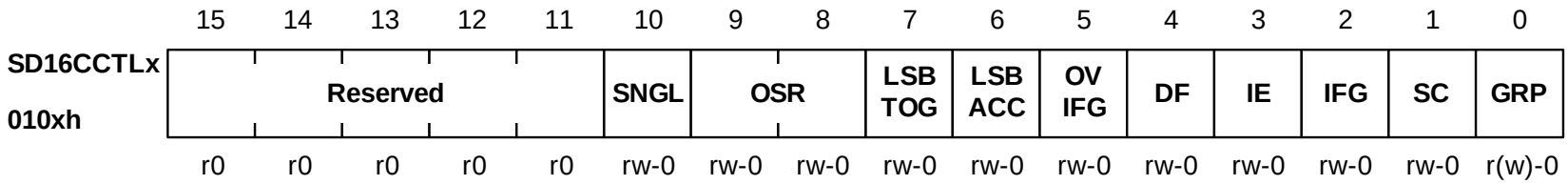
0 : MCLK

1 : SMCLK

2 : ACLK

3 : 外部时钟.

DIV 选择时钟分频系数. 1, 2 4 8



GRP 分组. (1:一个组的一部分, 0:一个组的结尾或者没用使用组)

SC 开始转换.

DF 数据格式化 (见 Sigma-Delta ADC 转换器 存储 寄存器 SD16MEMx)
(0: 无极性（无符号), 1:有极性（有符号）)

SD16CCTL0 |= GRP+SNGL+DF;

SD16CCTL1 |= GRP+SNGL+DF;

SD16CCTL2|=SNGL+DF;

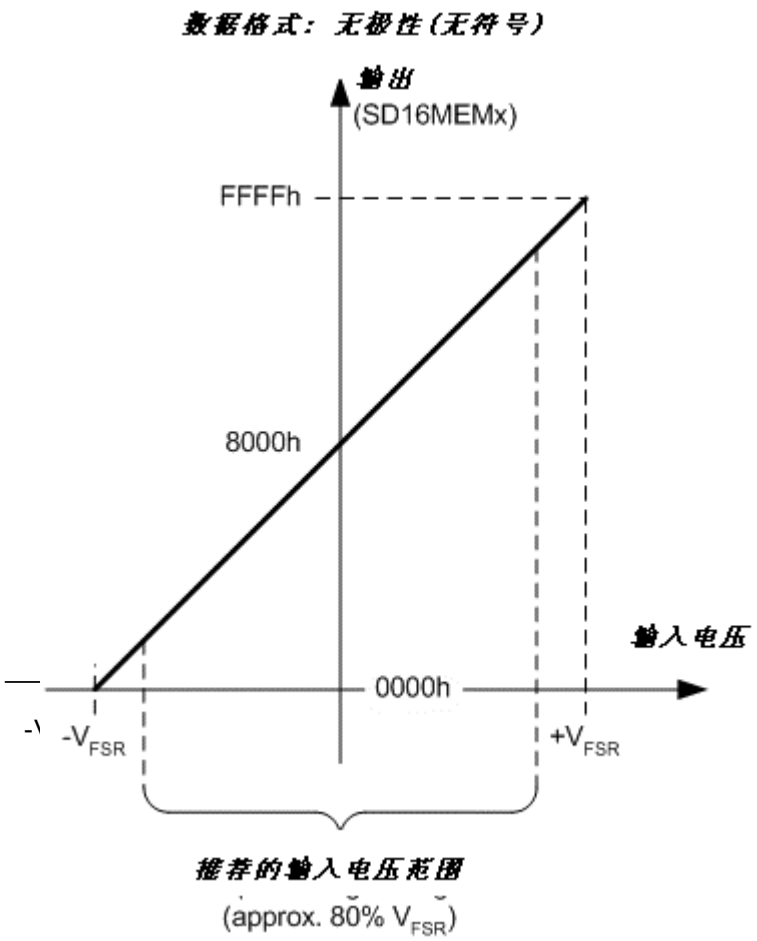
SNGL 信号转换.
0: 连续转换
1: 打开,推荐使用默认设置 (延迟3个采样)，以保证中断标志置位时得到一个正确的转换结果。

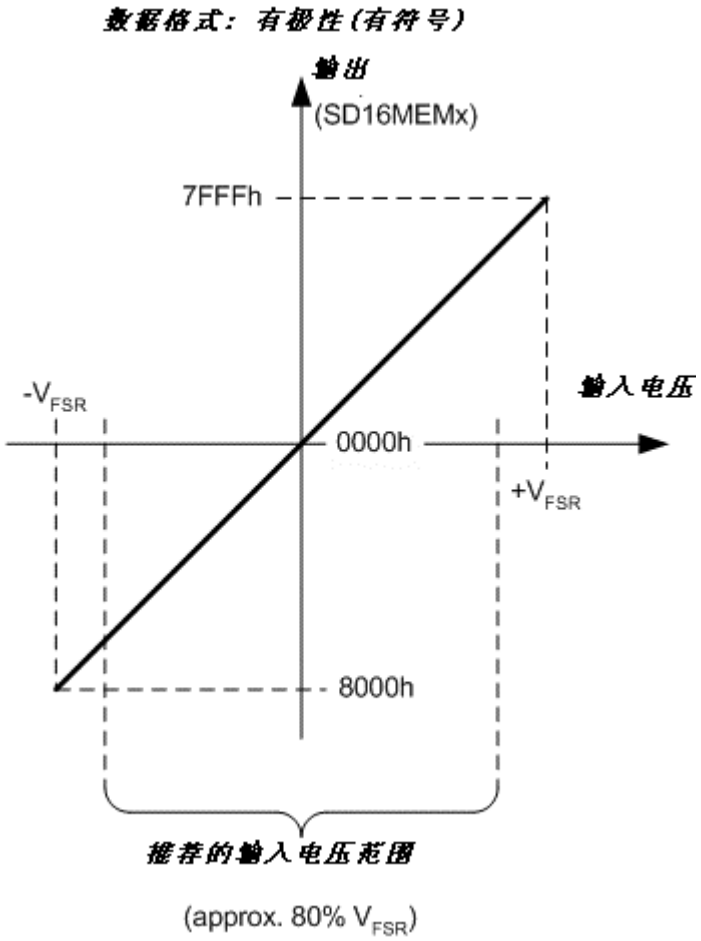
OSR 过采样率.
0: 256, 1:128, 2:64, 3:32

LSBACC 1: 数字过滤器的输出至少要有16个有效位.
0: 数字过滤器的输出最多有16个有效位.

LSBTOG 每次读SD16MEMx时，保持LSBACC的值不能改变

SD16 数字描述

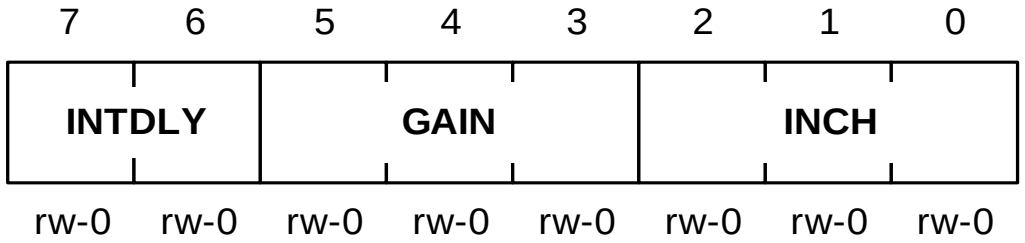

数据格式：无极性(无符号)
输出
(SD16MEMx)
FFFFh
8000h
0000h
输入电压
-V_FSR
+V_FSR
推荐的输入电压范围
(approx. 80% V_FSR)


数据格式：有极性(有符号)
输出
(SD16MEMx)
7FFFh
-V_FSR
0000h
输入电压
+V_FSR
8000h
推荐的输入电压范围
(approx. 80% V_FSR)

SD16 控制

SD16INCTLx

00Bxh



SD16INCTL0=INCH_0+GAIN_1;

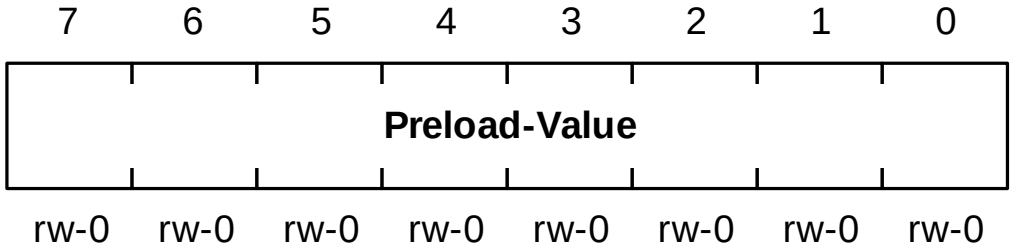
INCH　选择不同的输入通道.

GAIN　选择前置放大器的增益. 1,2,4,8,16,32

INTDLY　转换开始之前延迟的采样数: 3,2,1,0
这样可以使数字过滤器在产生数字（用于随后处理）之前先稳定下来

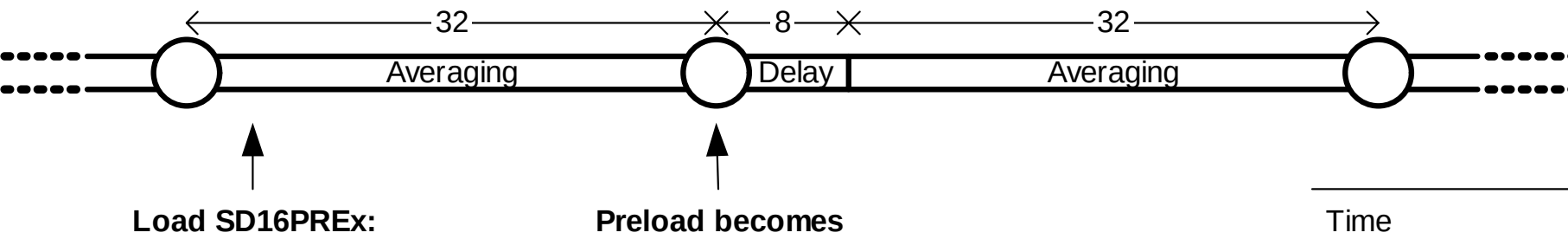
SD16PREx

00Bxh



SD16 相位转换寄存器

OSR = 32



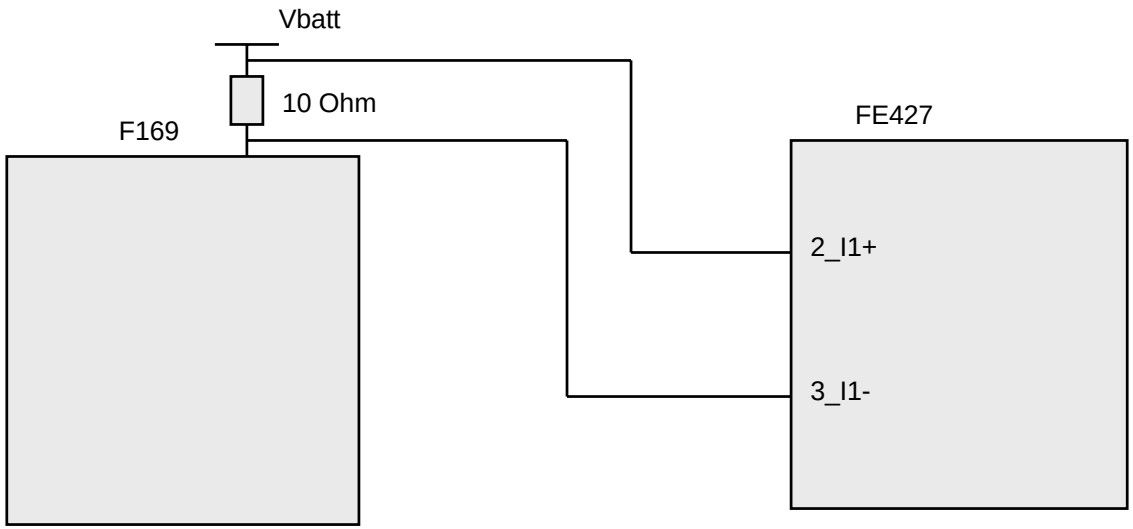
电压表和电流表的有效值计算

$$Vrms = \sqrt{\frac{\Sigma (V*V)}{N}} \cdot \frac{1.25V}{65536} \cdot \frac{1}{Gain}$$

$$Irms = \sqrt{\frac{\Sigma (V*V)}{N}} \cdot \frac{1.25V}{65536} \cdot \frac{1}{10} \cdot \frac{1}{Gain}$$

Project: WaveMachine (F169 演示板)

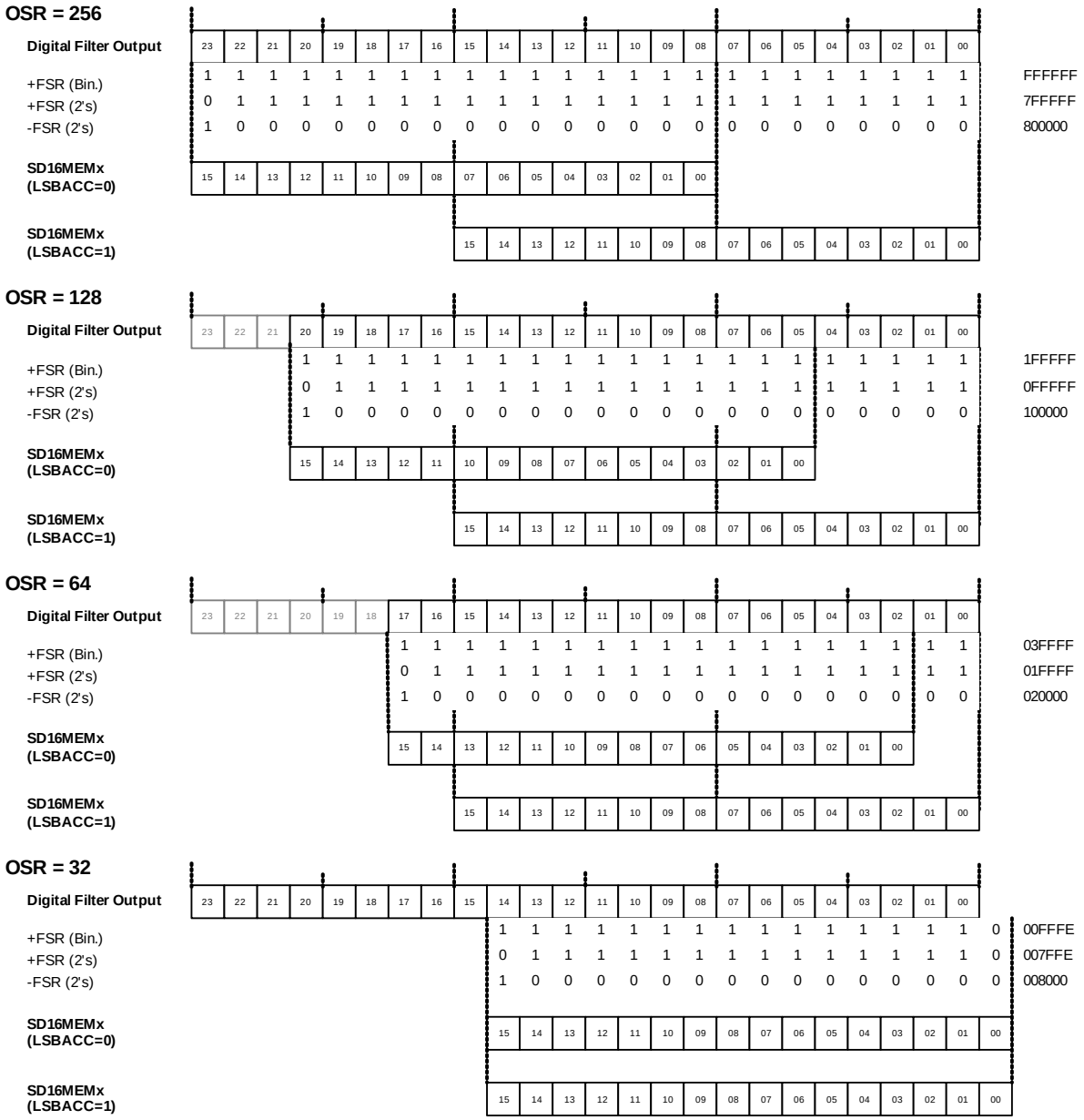
Project: AmpMeter (FE427 演示板)



SD16

OSR vs.

解析率



工程文件:称重仪 仿真

只适用于 VP430FE427